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Sir:

Transmitted herewith for filing is the patent application of Hyun-Eun Kim, Suk-Joong Lee, Gyu-Tae Hwang and Oh-Bong Kwon for **APPARATUS FOR CONVERTING ANALOG IMAGE DATA INTO DIGITAL IMAGE DATA IN CMOS IMAGE SENSOR**. The application comprises 11 pages, including specification, 6 claims, Abstract of the Disclosure, 4 sheets of drawings containing Figs. 1-4, and a Declaration and Power of Attorney.

Accompanying the application is the following:

- (1) A certified copy of Korean Application No. 1998-57237, filed December 22, 1998, the priority of which is claimed under 35 U.S.C. §119;

The Filing fee has been calculated as shown:

	No. <u>Filed</u>	No. <u>Extra</u>	<u>Small Entity</u>	<u>Other Than A Small Entity</u>
Basic Fee:			\$	\$ 760
Total claims: 6 - 20 = 0			x \$ 9 =	x \$ 18 = 0
Ind. claims: 1 - 3 = 0			x \$ 39 =	x \$ 78 = 0
Multiple claim presented			+ \$130 =	+ \$260 = 0
Assignment Recordation Fee			+ \$ 40 =	+ \$ 40 = 0
Non-English language			+ \$130 =	+ \$130 = 0
			<u>Total \$</u>	<u>Total \$ 760</u>



APPARATUS FOR CONVERTING ANALOG IMAGE DATA INTO DIGITAL IMAGE  
DATA IN CMOS IMAGE SENSOR

Field of the Invention

The present invention relates to a CMOS image sensor; and, more particularly, to an apparatus for converting an analog digital image data into a digital image data according to color characteristics.

Description of the prior Art

Generally, an image sensor is an apparatus to capture images using light sensing semiconductor materials. The image sensor includes a pixel array, which contains a plurality of image sensing elements, e.g., photodiode and receives light from an object to generate an electric image signal.

The image sensor includes a control and system interface unit for controlling the image sensor by controlling control signals, a pixel array and an analog-to-digital converter for converting an analog image data from the pixel array into a digital image data. Also, the analog-to-digital converter includes a ramp voltage generator for generating a reference voltage with a predetermined slope, a comparator for comparing the reference voltage with the analog image data to generate a digital image data, and a double buffer for storing the digital image data.

Fig. 2 is a circuit diagram illustrating a CMOS image sensor core. The core circuit includes a unit pixel 200, a comparator 320 and a unit latch circuit 400, and Fig. 3 is a plot illustrating an operation of a comparator and a double buffer shown in Fig. 2. That operation of the image sensor core is disclosed in a copending commonly owned application, U.S. Ser. No. 09/258,448, entitled "CMOS IMAGE SENSOR WITH TESTING CIRCUIT FOR VERIFYING OPERATION THEREOF" filed on Feb. 26, 1999. Therefore, a detailed description is omitted.

Using the conventional method for converting the analog image data into the digital image data, however, the analog-to-digital conversion operation is carried out only by comparing the reference voltage with the analog image data without consideration of color characteristics.

#### Summary of the Invention

It is, therefore, an object of the present invention to provide an apparatus for converting an analog digital image data into a digital image data in a CMOS image sensor according to color characteristics.

In accordance with an embodiment of the present invention, there is provided an apparatus for converting an analog image data into a digital image data in a CMOS image sensor including a pixel array having  $M(\text{row line}) \times N(\text{column line})$  color pixels, wherein the color pixels include a first color pixel for sensing a first color, a second color pixel for

sensing a second color and a third pixel for sensing a third color, the apparatus comprising: a) an analog reference voltage generating means for generating different analog reference voltages according to the color pixels, wherein the  
5 different analog reference voltage has different value and different decline rate; b) a selecting means, in response to a select control signal, for selecting one of the corresponding analog reference voltages according to the color pixels; and c) a comparing means for comparing the analog reference  
10 voltage and the analog image data to generate the digital image data corresponding to the color pixels, whereby a conversion operation of the analog image data into the digital image data is differently carried out according to the color characteristic.

#### Brief Description of the Drawings

Other objects and aspects of the invention will become apparent from the following description of the embodiments  
20 with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram illustrating a CMOS image sensor;

Fig. 2 is a circuit diagram illustrating a CMOS image sensor core;

25 Fig. 3 is a plot diagram illustrating an operation of a comparator and a double buffer; and

Fig. 4 is a block diagram illustrating a CMOS image

sensor according to the present invention.

#### Detailed Description of the Preferred Embodiments

5        Fig. 1 is a block diagram illustrating a CMOS image sensor. The CMOS image sensor includes a control and system interface unit 10, a pixel array 20 having a plurality of image sensing elements, and an analog-to-digital converter 30. The analog-to-digital converter 30 also a ramp voltage generator 31 for generating a reference voltage, a comparator 32 for comparing the reference voltage with a analog image data from the pixel array 20 to generator a digital image data, and a double buffer 40 for storing the digital image data.

10        In this present invention, the analog-to-digital conversion is modified as shown in Fig. 4.

15        Fig. 4 is a block diagram illustrating a CMOS image sensor according to the present invention. Referring to Fig. 4, a CMOS image sensor includes a pixel array 50 of Bayer pattern type includes MxN color pixels, arranged in a matrix, and an analog-to-digital conversion unit 60 for converting an analog image data into a digital image data.

20        The pixel array 50 of Bayer pattern type is incorporated with repetitive arrangements of a RGRG type and a GBGB type in odd row lines and even row lines line, respectively. Here, "R" represents a red color pixel for sensing only red color, "G" a green color pixel for sensing only green color and "B" a blue color pixel for sensing blue color. Each analog voltage

signal corresponding to respective color pixels has a different characteristic. By employing the different color characteristic, the analog-to-digital converter generates a different reference voltage at the analog-to-digital conversion to convert an analog image data into a digital image data.

The analog-to-digital conversion unit 60 includes analog reference voltage generating units 601A, 601B and 601C, N multiplexers 602A and 602B, and N comparators 603A and 603B. Here, the analog reference voltage generating units includes a first reference voltage generator 601A for the blue color pixel, a second reference voltage generator 601B for the green color pixel, and a third reference voltage generator 601C for the red color pixel, each of which generates respective analog reference voltage with a different decline rate. The multiplexers 602A and 602B selectively output one of the analog reference voltages in response to a select control signal SEL and the comparators 603A and 603B compare the selected reference voltage from the multiplexers 602A and 602B with the analog image data from the pixel array 50. At this point, since red pixels and green pixels are arranged on odd column lines by turns, the multiplexers 602A arranged on the odd column lines output one of the analog reference voltage of the second and third reference voltage generators 602B and 601C according to the color pixels. On the contrary, since green pixels and blue pixels are arranged on even column lines by turns, the multiplexers 602B arranged on even lines output

one of the analog reference voltages of the first and second reference voltage generators 601A and 601B according to the color pixels.

5 First, the conversion operation at the first row line will be described.

10 Since the red pixels and the green pixels are arranged on the odd column lines and the even column lines, respectively, the multiplexers 602A arranged on the odd column lines selectively output the analog reference voltage of the third reference generator 601C in response to the select control signal SEL to the comparators 603A arranged on the odd column line. Also, the multiplexers 602B arranged on the even column lines selectively output the reference voltage of the second reference generator 601B in response to the select control signal SEL to the comparator 603B arranged on the even column lines. Then, the comparators 603A arranged on the odd column lines compare the analog image data from the red pixels with the output of the multiplexers 602A. In similar manner, the comparators 603B arranged on the even column lines compare the analog image data from the green pixels with the output of the multiplexers 602B. Then, the following procedure is the same as the prior art.

25 Next, a conversion operation at the second row line will be described.

Since the green pixels and the blue pixels are arranged on the odd column lines and the even column lines, respectively, the multiplexers 602A arranged on the odd column

lines selectively output the analog reference voltage of the second reference generator 601C in response to the select control signal SEL to the comparators 603A arranged on the odd column line. Also, the multiplexers 602B arranged on the even  
5 column lines selectively output the reference voltage of the first reference generator 601B in response to the select control signal SEL to the comparator 603B arranged on the even column lines. Then, the comparators 603A arranged on the odd column lines compare the analog image data from the green  
10 pixels with the output of the multiplexers 602A. In similar manner, the comparators 603B arranged on the even column lines compare the analog image data from the blue pixels with the output of the multiplexers 602B. Then, the following procedure is the same as the prior art.

15 By carrying out the above-mentioned operation repeatedly, analog image data of all of the color pixels can be converted into corresponding digital image data.

Since different analog reference voltages are generated according to the image data characteristic, the red, green and  
20 blue color characteristics can be precisely controlled.

While the present invention has been described with respect to certain preferred embodiments only, other modifications and variation may be made without departing from the spirit and scope of the present invention as set forth in  
25 the following claims.



What is claimed is:

1. An apparatus for converting an analog image data into a digital image data in a CMOS image sensor including a pixel array having M(row line) $\times$ N(column line) color pixels, wherein the color pixels include a first color pixel for sensing a first color, a second color pixel for sensing a second color and a third pixel for sensing a third color, the apparatus comprising:

a) an analog reference voltage generating means for generating different analog reference voltages according to the color pixels, wherein the different analog reference voltage has different value and different decline rate;

b) a selecting means, in response to a select control signal, for selecting one of the corresponding analog reference voltages according to the color pixels; and

c) a comparing means for comparing the analog reference voltage and the analog image data to generate the digital image data corresponding to the color pixels,

whereby a conversion operation of the analog image data into the digital image data is differently carried out according to the color characteristic.

2. The apparatus as recited in claim 1, wherein the analog reference voltage generating means includes:

a first reference voltage generator for generating a first reference voltage with respect to the first color pixel;

a second reference voltage generator for generating a second reference voltage with respect to the second color pixel; and

a third reference voltage generator for generating a  
5 third reference voltage with respect to the third color pixel.

3. The apparatus as recited in claim 2, wherein the color pixels contained in the pixel array are arranged as a form of Bayer pattern, the Bayer pattern including:

10 the first color pixels and the second color pixels repeatedly arranged on odd row lines of the pixel array in this order;

and the second color pixels and the third color pixels repeatedly arranged on even row lines of the pixel array in  
15 this order.

4. The apparatus as recited in claim 3, wherein the selecting means includes:

a first selecting means, arranged on the odd column lines,  
20 for selecting one of the first reference voltage and the second reference voltage in response to the select control signal according to the color pixels; and

a second selecting means, arranged on the even column lines, for selecting one of the second reference voltage and  
25 third reference voltage in response to the select control signal according to the color pixels.

5. The apparatus as recited in claim 4, wherein the first color pixel is a red color pixel, the second color pixel is a green color pixel and the third color pixel is a blue color pixel.

5

6. The apparatus as recited in claim 4, wherein the selecting means is a multiplexer.

## Abstract of the Disclosure

Disclosed is an apparatus for converting an analog image  
5 data into a digital image data in a CMOS image sensor  
including a pixel array having  $M(\text{row line}) \times N(\text{column line})$   
color pixels, wherein the color pixels include a first color  
pixel for sensing a first color, a second color pixel for  
sensing a second color and a third pixel for sensing a third  
10 color. The apparatus includes an analog reference voltage  
generating unit for generating different analog reference  
voltages according to the analog image data of the color  
pixels, wherein the different analog reference voltage has  
different value and different decline rate, a selecting unit,  
15 in response to a select control signal, for selecting one of  
the corresponding analog reference voltages according to the  
color pixels, and a comparing unit for comparing the analog  
reference voltage and the analog image data to generate the  
digital image data corresponding to the color pixels, whereby  
20 a conversion operation of the analog image data into the  
digital image data is differently carried out according to the  
color characteristic.

FIG. 1

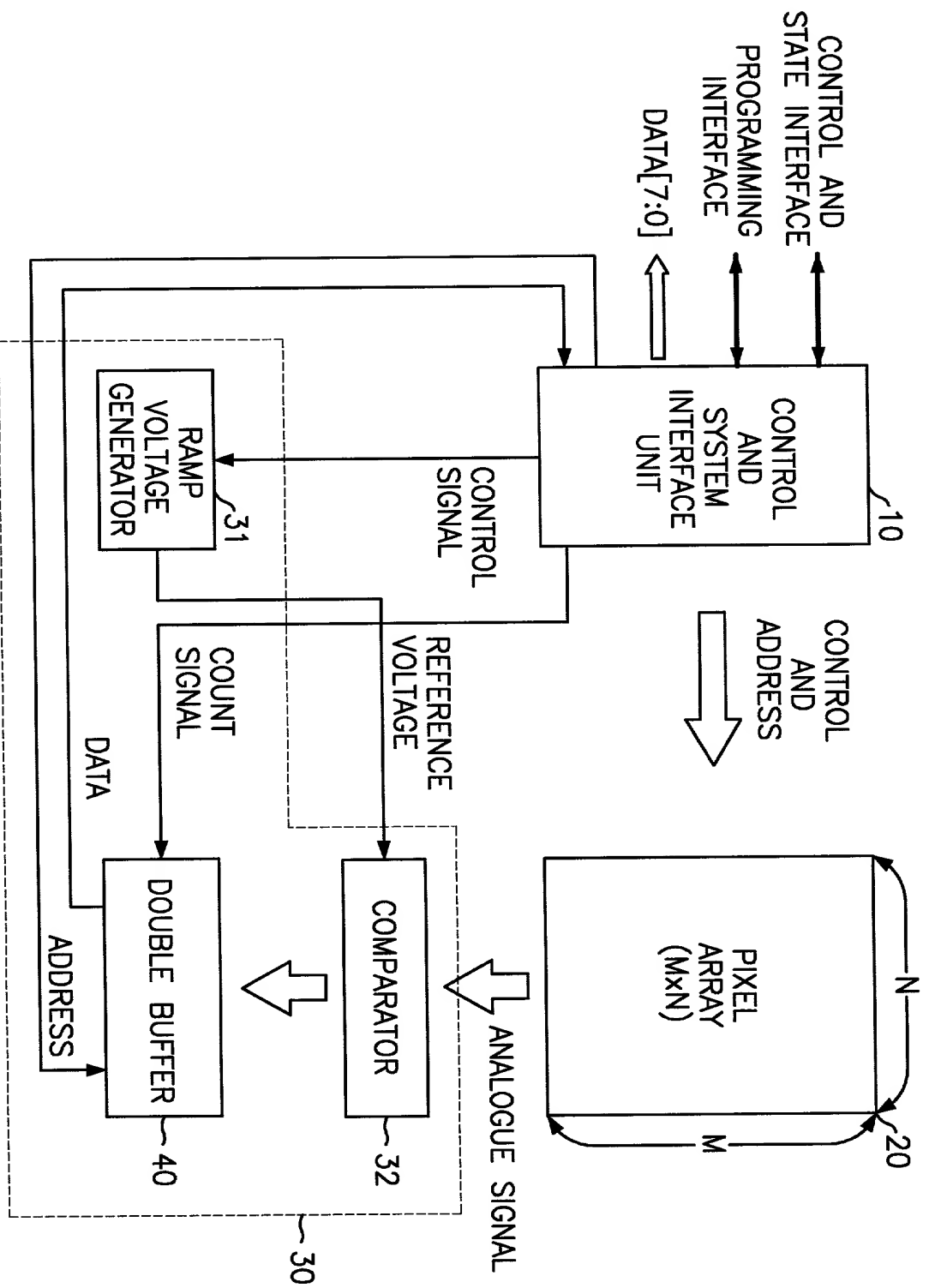


FIG. 2  
(PRIOR ART)

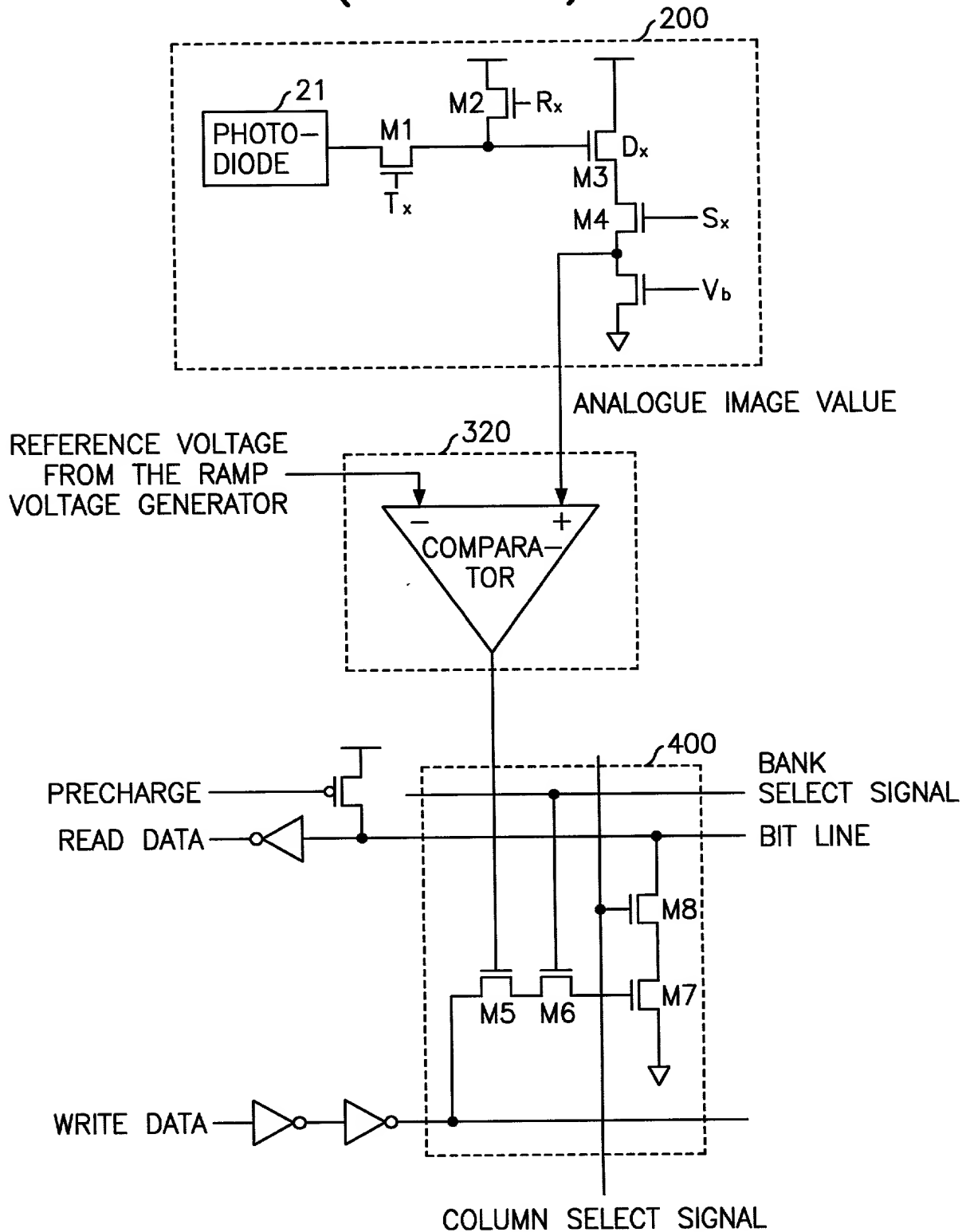


FIG. 3

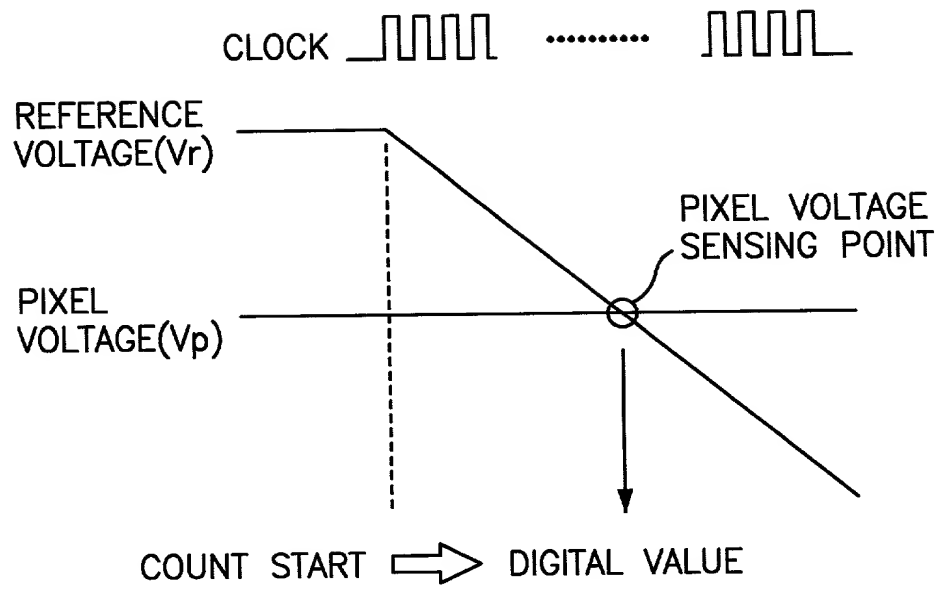
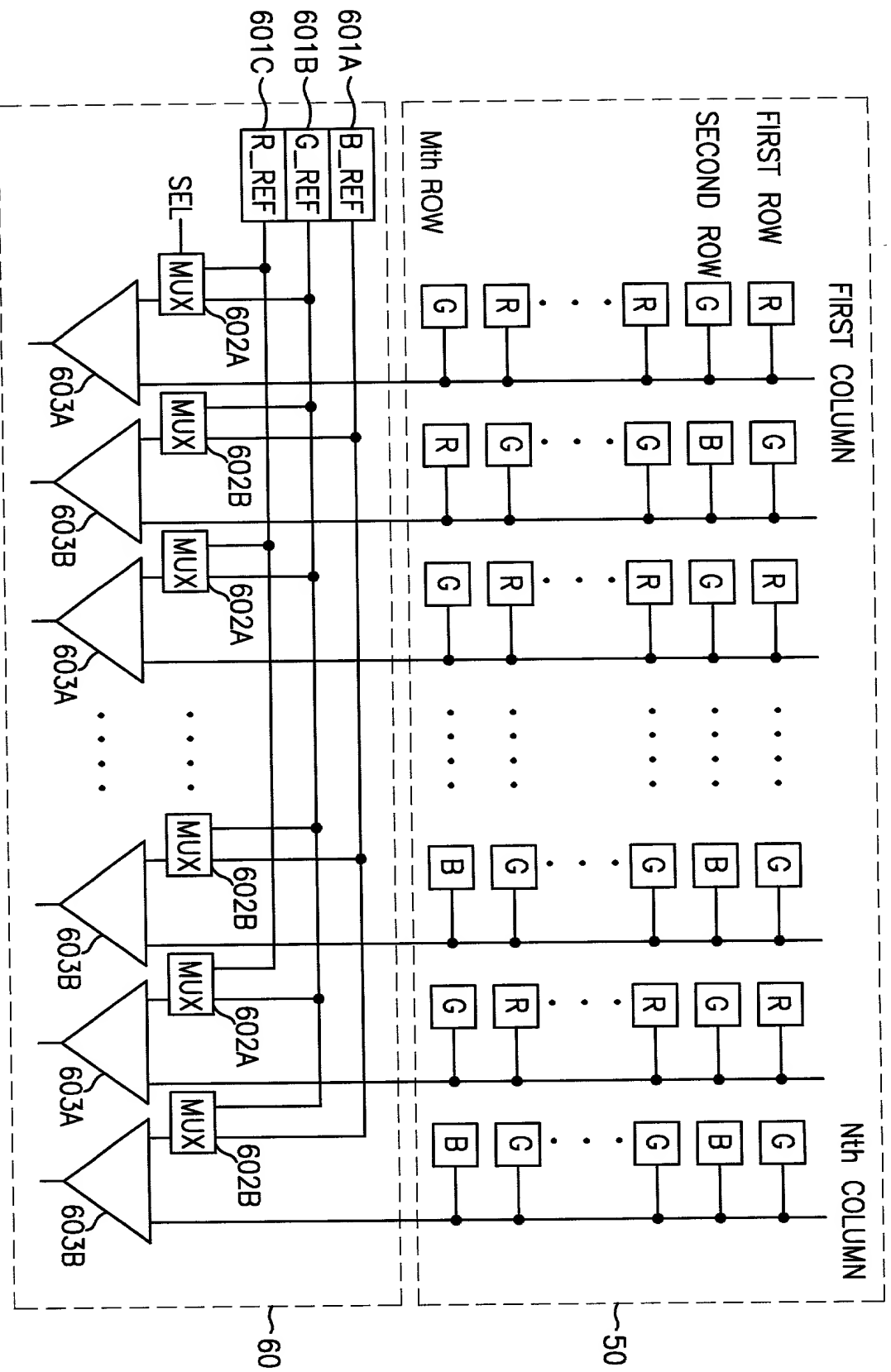


FIG. 4





DECLARATION  
AND POWER OF ATTORNEY  
U.S.A.

FOR ATTORNEY'S USE ONLY

ATTORNEYS' DOCKET NO.

ALL PATENTS, INCLUDING DESIGN  
FOR APPLICATION BASED ON PCT; PARIS CONVENTION;  
NON PRIORITY; OR PROVISIONAL APPLICATIONS

As a below named inventor, I declare that my residence, post office address and citizenship are stated below next to my name, the information given herein is true, that I believe that I am the original, first and sole inventor (if only one name is listed at 201 below), or an original, first and joint inventor (if plural inventors are named below at 201-203, or on additional sheets attached hereto) of the subject matter which is claimed and for which patent is sought on the invention entitled:

APPARATUS FOR CONVERTING ANALOG IMAGE DATA INTO DIGITAL IMAGE DATA

IN CMOS IMAGE SENSOR

which is described and claimed in:

☐ PCT international Application No. \_\_\_\_\_ filed \_\_\_\_\_

☒ the attached specification

☐ the specification in application Serial No. \_\_\_\_\_ filed \_\_\_\_\_

(if applicable) and amended on \_\_\_\_\_

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a)-(b) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

Priority Claimed

1998-57237  
(Number)

Republic of Korea  
(Country)

22/12/1998  
(Day/Month/Year Filed)

☒ Yes  
☐ No

(Number)

(Country)

(Day/Month/Year Filed)

☐ Yes  
☐ No

(Number)

(Country)

(Day/Month/Year Filed)

☐ Yes  
☐ No

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Application No. \_\_\_\_\_ Filing Date \_\_\_\_\_ Application No. \_\_\_\_\_ Filing Date \_\_\_\_\_

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)

(Filing Date)

(Status: patented, pending, abandoned)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorneys(Registration No.) to prosecute this application, receive and act on instructions from my agent, and transact all business in the Patent and Trademark Office connected therewith. HARVEY B. JACOBSON, JR.(20,851); D. DOUGLAS PRICE (24,514); JOHN CLARKE HOLMAN (22,769); MARVIN R. STERN (20,640); MICHAEL R. SLOBASKY (26,421); JONATHAN L. SCHERER (29,851); IRWIN M. AISENBERG (19,007); WILLIAM E. PLAYER (31,409); Yoon S. Ham (45,307)

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	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE OR COUNTRY

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under section 1001 of Title 18 of the United States Code; and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201\*

SIGNATURE OF INVENTOR 202\*

SIGNATURE OF INVENTOR 203\*

DATE Nov. 15, 1999

DATE Nov. 15, 1999

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**ADDITIONAL INVENTORS**

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	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE	
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	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE	

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under section 1001 of Title 18 of the United States Code; and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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DATE <b>Nov. 15, 1999</b>	DATE	DATE
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DATE	DATE	DATE
SIGNATURE OF INVENTOR 210*	SIGNATURE OF INVENTOR 211*	
DATE	DATE	